REMARKS

This reply is responsive to the Office Action mailed on May 22, 2006. Claims 1-32 are pending in the application. Claims 1-17 are canceled without prejudice. Reconsideration in light of the following remarks is respectfully requested.

I. Objection to the Drawings

Corrected drawings are provided as required by the Examiner.

II. Objection to the Specification

The Specification has been amended to include the application no. and filing date of the co-pending application as required by the Examiner.

III. Rejections under 35 U.S.C. § 101

Claims 1-32 stand rejected under 35 U.S.C. § 101. Applicants respectfully disagree.

Claims 1-17 are canceled without prejudice by this Response, rendering their rejection moot. As stated by the Examiner, in order for claims to be statutory, claims must either include a practical application, or a discrete, useful and tangible result. Here, claims 18-32 comply with 35 U.S.C. § 101 at least because independent claims 18, 31, and 32 involve obtaining an approximate packed value result, which is then used to determine FIR filter operations. Independent claims 18, 31, and 32 clearly recite more

than "performing average of two numbers" as argued by the Examiner. Withdrawal of the rejection is respectfully requested.

Applicants also traverse the Examiner's assertion that the computer readable medium is not tangible. Applicants respectfully request that the Examiner prove why paragraph [141] of Applicants' Specification, in the Examiner's opinion, does not show a tangible computer readable medium.

IV. Rejections under 35 U.S.C. § 103

A. Claims 1-32

Claims 1-32 stand rejected under 35 U.S.C. § 103(a) as being obvious over Dijkstra (U.S. Patent No. 6,795,841) in view of Nagano et al. (U.S. Patent No. 6,084,907) (Nagano). Applicants respectfully disagree.

Claims 1-17 are canceled without prejudice by the Response thereby rendering their rejection moot.

Dijkstra discloses that when performing data processing operations upon data words 2, 4 including a plurality of abutting data values a0, a1, a2, a3, b0, b1, b2 and b3 the results of the operation upon one data value may influence a neighboring data value in an undesired manner. An error correcting value 34 may be determined from the input data words 2, 4 and then combined with the intermediate result 32 to correct for any undesired interactions between adjacent data values. (Dijkstra, Abstract)

Nagano discloses automatically amending a signal distorted through propagation in a transmission line to the expected value, each multiplication unit includes a plurality

of weight coefficient holding units for storing weight coefficients. The number of these weight coefficient holding units is the same as the clock number which is equal to a delay required for updating the weight coefficients. An adder calculates weight coefficients every clock. The storage location of the calculated weight coefficients is switched by a selector, and the weight coefficients calculated every clock are serially held in a corresponding one of the weight coefficient holding units. The other selectors serially select one of the plurality of weight coefficient holding units and the weight coefficients thus held are given to the multiplication units. Consequently, each of the weight coefficients held in the weight coefficient holding units is given to a corresponding one of the multiplication units in a time period corresponding to the clock number equal to the delay time required for updating the weight coefficients. Thus, even if there is a delay before the update of the weight coefficients, an output error does not diverge, which makes it possible to obtain an ideal output signal in a short time and in a stable manner. (Abstract)

The Examiner's attention is directed to the fact that Dijkstra and Nagano fail to disclose "using the SIMD instruction on a plurality of packed values to obtain an approximate packed value result", as recited in independent claims 18, 31, and 32.

The Examiner argues that Dijkstra teaches the use of a SIMD instruction. Dijkstra notes the existence of SIMD, however, Dijkstra actually *teaches away* from the use of SIMD. As can be seen from the passage of Dijkstra illustrated below, Dijkstra illustrates the *disadvantages* of using single instruction multiple data (SIMD) instructions.

> Whilst the provision of single instruction multiple data instructions does allow advantageous parallel processing of data values within a single data word, it suffers from the disadvantage that it occupies bit space within the instruction bit space of the data processing apparatus concerned and requires the provision of extra circuitry. Instruction bit space is a valuable resource within a data processing system architecture and increased circuit requirements increase cost, size, power consumption etc. A further disadvantage of the single instruction multiple data instruction approach is that the divisions between data values within a data word are determined by the hardware of the system which gives reduced flexibility in the way the system may be used, e.g. the hardware may assume that the data values are 16-bit data values with two data values being stored within a 32-bit data word, whereas a particular processing requirement might be to handle 8-bit data values, which make relatively inefficient use of a 16-bit data channel provided for them within the single instruction multiple data arrangement. (Dijkstra, column 1, lines 36-55)

Similarly, Nagano is devoid of the teaching, disclosure or suggestion of using SIMD instructions. Applicants' review of Nagano failed to produce any teaching or suggestion of using SIMD instructions.

Applicants respectfully request that the Examiner explain how Dijkstra teaches Applicants invention as recited in claims 18-32. Specifically, Applicants respectfully request the Examiner to show how Dijkstra in view of Nagano teaches the Applicants invention when Dijkstra teaches away from using SIMD and Nagano is completely devoid of the teaching, disclosure, or suggestion of SIMD.

In light of the above arguments, Applicants assert that independent claims 18, 31, and 32 are patentable over Dijkstra in view of Nagano. As such, claims 19-30 are patentable at least by virtue of depending either directly or indirectly from independent claim 18.

B. Claims 15, 16, 19, 20, and 30

Claims 15, 16, 19, 20, and 30 stand rejected under 35 U.S.C. § 103(a) as being obvious over Dijkstra and Nagano in view of Applicants' Specification. Applicants respectfully disagree.

The Examiner concedes that Dijkstra in view of Nagano fails to disclose the PAVG function. The Examiner points to Applicants' Specification in order to cure the Examiner's perceived deficiencies of the cited art.

As stated above in Section IV. A., Dijkstra and Nagano fail to teach "using the SIMD instruction on a plurality of packed values to obtain an approximate packed value result", as recited in independent claims 18, 31, and 32. The Examiner's citation to the Applicants Specification does not cure this deficiency. As such, the combination of Dijkstra and Nagano fails to render claims 15, 16, 19, 20, and 30 obvious. Therefore, claims 15, 16, 19, 20, and 30 are patentable over Dijkstra and Nagano.

Conclusion

Having fully responded to the Office action, the application is believed to be in condition for allowance. Should any issues arise that prevent early allowance of the above application, the examiner is invited contact the undersigned to resolve such issues.

To the extent an extension of time is needed for consideration of this response, Applicant hereby request such extension and, the Commissioner is hereby authorized to charge deposit account number 502117 for any fees associated therewith.

Date: 11/22/2006

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